8-Bit, High Speed, Multiplying D/A Converter (Universal Digital Logic Interface)

DAC08

FEATURES
Fast Settling Output Current: 85 ns
Full-Scale Current Prematched to ±1 LSB
Direct Interface to TTL, CMOS, ECL, HTL, PMOS
Nonlinearity to 0.1% Maximum Over Temperature Range
High Output Impedance and Compliance: –10 V to +18 V
Complementary Current Outputs
Wide Range Multiplying Capability: 1 MHz Bandwidth
Low FS Current Drift: ±10 ppm/°C
Wide Power Supply Range: ±4.5 V to ±18 V
Low Power Consumption: 33 mW @ ±5 V
Low Cost
Available in Die Form

GENERAL DESCRIPTION

The DAC08 series of 8-bit monolithic digital-to-analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic input.

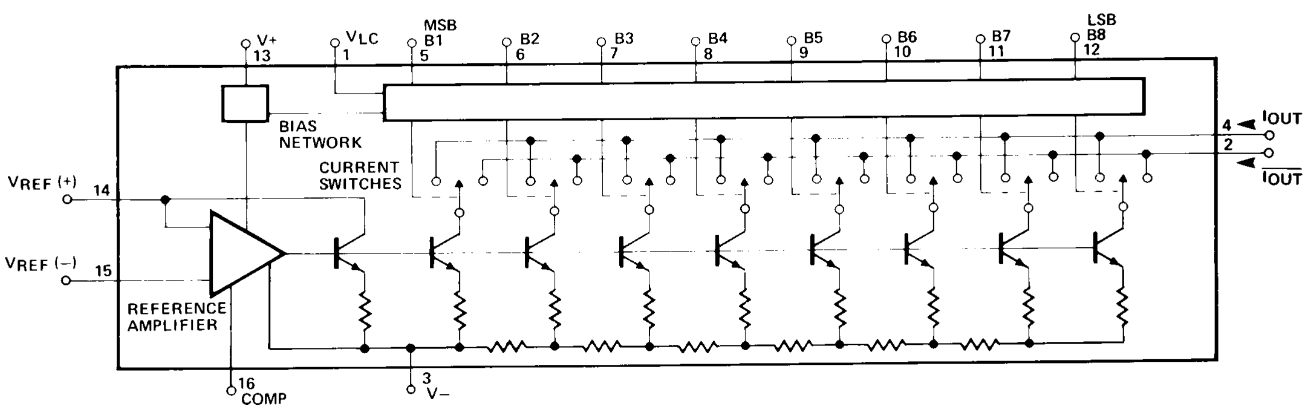
High voltage compliance complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5 V to ±18 V power supply range, with 33 mW power consumption attainable at ±5 V supplies.

The compact size and low power consumption make the DAC08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC08 applications include 8-bit, 1 µs A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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DAC08–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, I_{REF} = 2.0 mA, –55°C ≤ T_A ≤ +125°C for DAC08/08A, 0°C ≤ T_A ≤ +70°C for DAC08C, E & H unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	DAC08A/H Min	DAC08A/H Typ	DAC08A/H Max	DAC08E Min	DAC08E Typ	DAC08E Max	DAC08C Min	DAC08C Typ	DAC08C Max	Units
Resolution			8			8			8			Bits
Monotonicity			8			8			8			Bits
Nonlinearity	NL				±0.1			±0.19			±0.39	% FS
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, T_A = 25°C[1]		85	135		85	150		85	150	ns
Propagation Delay												
Each Bit	t_{PLH}	T_A = 25°C[1]		35	60		35	60		35	60	ns
All Bits Switched	t_{PHL}			35	60		35	60		35	60	ns
Full-Scale Tempco[1]	TCI_{FS}			±10	±50		±10	±80		±10	±80	ppm/°C
		DAC08E						±50				
Output Voltage Compliance (True Compliance)	V_{OC}	Full-Scale Current Change <1/2 LSB, R_{OUT} > 20 MΩ typ	–10		+18	–10		+18	–10		+18	V
Full Range Current	I_{FR4}	V_{REF} = 10.000 V R14, R15 = 5.000 kΩ T_A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR4} – I_{FR2}$		±0.5	±4		±1	±8		±2	±16	µA
Zero-Scale Current	I_{ZS}			0.1	1		0.2	2		0.2	4	µA
Output Current Range	I_{OR1}	R14, R15 = 5.000 kΩ	2.1			2.1			2.1			mA
	I_{OR2}	V_{REF} = +15.0 V, V– = –10 V										
		V_{REF} = +25.0 V, V– = –12 V	4.2			4.2			4.2			mA
Output Current Noise		I_{REF} = 2 mA		25			25			25		nA
Logic Input Levels												
Logic "0"	V_{IL}	V_{LC} = 0 V			0.8			0.8			0.8	V
Logic Input "1"	V_{IL}		2			2			2			V
Logic Input Current		V_{LC} = 0 V										
Logic "0"	I_{IL}	V_{IN} = –10 V to +0.8 V		–2	–10		–2	–10		–2	–10	µA
Logic Input "1"	I_{IH}	V_{IN} = 2.0 V to 18 V		0.002	10		0.002	10		0.002	10	µA
Logic Input Swing	V_{IS}	V– = –15 V	–10		+18	–10		+18	–10		+18	V
Logic Threshold Range	V_{THR}	V_S = ±15 V[1]	–10		+13.5	–10		+13.5	–10		+13.5	V
Reference Bias Current	I_{15}			–1	–3		–1	–3		–1	–3	µA
Reference Input Slew Rate	dI/dt	R_{EQ} = 200 Ω R_L = 100 Ω C_C = 0 pF	4	8		4	8		4	8		mA/µs
		See Fast Pulsed Ref. Info Following.[1]										
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = 4.5 V to 18 V		±0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%ΔI$_O$/%ΔV+
	$PSSI_{FS–}$	V– = –4.5 V to –18 V I_{REF} = 1.0 mA		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	%ΔI$_O$/%ΔV–
Power Supply Current	I+	V_S = ±5 V, I_{REF} = 1.0 mA		2.3	3.8		2.3	3.8		2.3	3.8	mA
	I–			–4.3	–5.8		–4.3	–5.8		–4.3	–5.8	mA
	I+	V_S = +5 V, –15 V,		2.4	3.8		2.4	3.8		2.4	3.8	mA
	I–	I_{REF} = 2.0 mA		–6.4	–7.8		–6.4	–7.8		–6.4	–7.8	mA
	I+	V_S = ±15 V, I_{REF} =		2.5	3.8		2.5	3.8		2.5	3.8	mA
	I–	2.0 mA		–6.5	–7.8		–6.5	–7.8		–6.5	–7.8	mA
Power Dissipation	P_d	±5 V, I_{REF} = 1.0 mA		33	48		33	48		33	48	mW
		+5 V, –15 V, I_{REF} = 2.0 mA		108	136		103	136		108	136	mW
		±15 V, I_{REF} = 2.0 mA		135	174		135	174		135	174	mW

NOTES
[1]Guaranteed by design.

Specifications subject to change without notice.

TYPICAL ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, and I_{REF} = 2.0 mA, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	All Grades Typical	Units
Reference Input Slew Rate	dI/dt		8	mA/µs
Propagation Delay	t_{PLH}, t_{PHL}	T_A = 25°C, Any Bit	35	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, T_A = 25°C	85	ns

NOTES
For DAC08NT & GT 25°C characteristics, see DAC08N & G characteristics respectively.
Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]

Operating Temperature
- DAC08AQ, Q . . . . –55°C to +125°C
- DAC08HQ, EQ, CQ, HP, EP, CP, CS . . . . . 0°C to +70°C

Junction Temperature (T_J) . . . . –65°C to +150°C
Storage Temperature Q Package . . . . –65°C to +150°C
Storage Temperature P Package . . . . –65°C to +125°C
Lead Temperature (Soldering, 60 sec) . . . . 300°C
V+ Supply to V– Supply . . . . 36 V
Logic Inputs . . . . V– to V– plus 36 V
V_{LC} . . . . V– to V+
Analog Current Outputs (at V_S– = 15 V) . . . . 4.25 mA
Reference Input (V_{14} to V_{15}) . . . . V– to V+
Reference Input Differential Voltage
- (V_{14} to V_{15}) . . . . ±18 V

Reference Input Current (I_{14}) . . . . 5.0 mA

Package Type	θ_{JA}[2]	θ_{JC}	Units
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	76	36	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

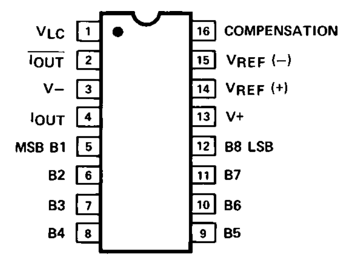
ORDERING GUIDE[1]

NL	16-Pin Dual-In-Line Package Hermetic	Plastic	LCC	Operating Temperature Range
0.1%	DAC08AQ[2]			MIL
	DAC08HQ	DAC08HP		COM
0.19%	DAC08Q[2]		DAC08RC/883	MIL
	DAC08EQ	DAC08EP		COM
0.39%	DAC08CQ	DAC08CP		COM
		DAC08CS[3]		COM

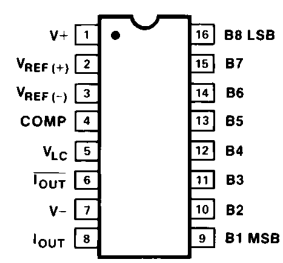
NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
[3]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS

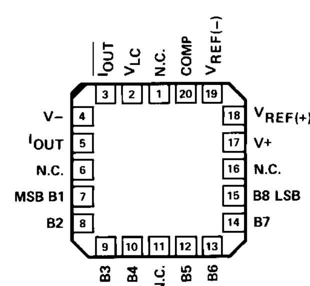
16-Pin Dual-In-Line Package (Q Suffix)



16-Lead SO (S Suffix)



DAC08RC/883 20-Lead LCC (RC Suffix)



NC = NO CONNECT

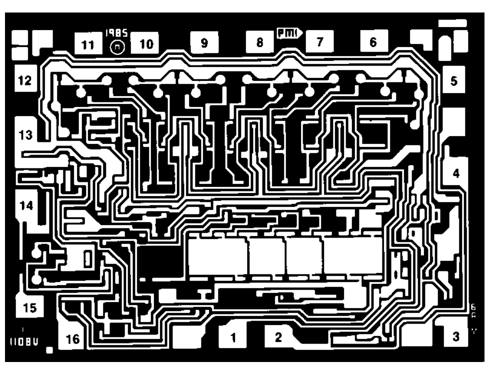
WAFER TEST LIMITS (@ V_S = ±15 V, I_{REF} = 2.0 mA, T_A = 125°C for DAC08NT, DAC08GT devices; T_A = 25°C for DAC08N, DAC08G and DAC08GR devices, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	DAC08NT Limit	DAC08N Limit	DAC08GT Limit	DAC08G Limit	DAC08GR Limit	Units
Resolution			8	8	8	8	8	Bits min
Monotonicity			8	8	8	8	8	Bits min
Nonlinearity	NL		±0.1	±0.1	±0.19	±0.19	±0.39	% FS max
Output Voltage	V_{OC}	Full-Scale Current	+18	+18	+18	+18	+18	V max
Compliance		Change < 1/2 LSB	–10	–10	–10	–10	–10	V min
Full-Scale Current	I_{FS4} or	V_{REF} = 10.000 V	2.04	2.04	2.04	2.04	2.04	mA max
	I_{FS2}	R_{14}, R_{15} = 5.000 kΩ	1.94	1.94	1.94	1.94	1.94	mA min
Full-Scale Symmetry	I_{FSS}		±8	±8	±8	±8	±16	µA max
Zero-Scale Current	I_{ZS}		2	2	4	4	4	µA max
Output Current Range	I_{FS1}	V– = –10 V,						
		V_{REF} = +15 V	2.1	2.1	2.1	2.1	2.1	mA min
		V– = –12 V,						
	I_{FS2}	V_{REF} = +25 V	4.2	4.2	4.2	4.2	4.2	mA min
		R_{14}, R_{15} = 5.000 kΩ						
Logic Input "0"	V_{IL}		0.8	0.8	0.8	0.8	0.8	V max
Logic Input "1"	V_{IH}		2	2	2	2	2	V min
Logic Input Current		V_{LC} = 0 V						
Logic "0"	I_{IL}	V_{IN} = –10 V to +0.8 V	±10	±10	±10	±10	±10	µA max
Logic "1"	I_{IH}	V_{IN} = 2.0 V to 18 V	±10	±10	±10	±10	±10	µA max
Logic Input Swing	V_{IS}	V– = –15 V	+18	+18	+18	+18	+18	V max
			–10	–10	–10	–10	–10	V min
Reference Bias Current	I_{15}		–3	–3	–3	–3	–3	µA max
Power Supply	$PSSI_{FS+}$	V+ = 4.5 V to 18 V	0.01	0.01	0.01	0.01	0.01	% FS/% V max
Sensitivity	$PSSI_{FS-}$	V– = –4.5 V to –18 V						
		I_{REF} = 1.0 mA						
Power Supply Current	I+	V_S = ±15 V	3.8	3.8	3.8	3.8	3.8	mA max
		I_{REF} ≤ 2.0 mA	–7.8	–7.8	–7.8	–7.8	–7.8	µA max
Power Dissipation	P_d	V_S = ±15 V	174	174	174	174	174	mW max
		I_{REF} ≤ 2.0 mA						

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

DICE CHARACTERISTICS

(+125°C Tested Dice Available)



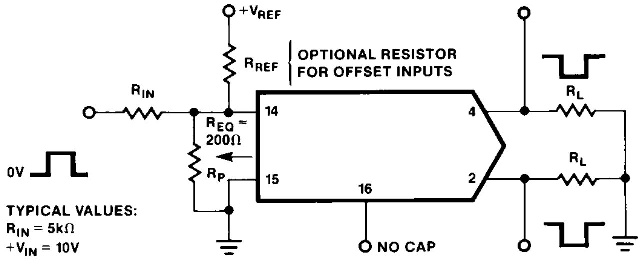


Figure 1. Pulsed Reference Operation

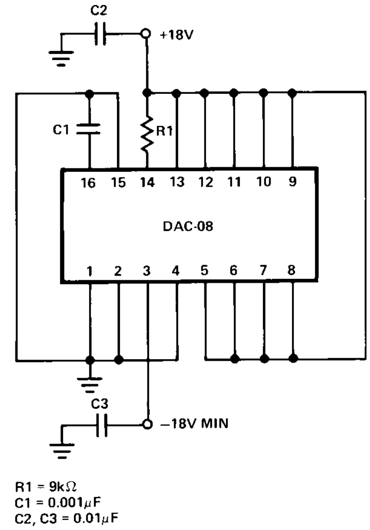


Figure 2. Burn-in Circuit

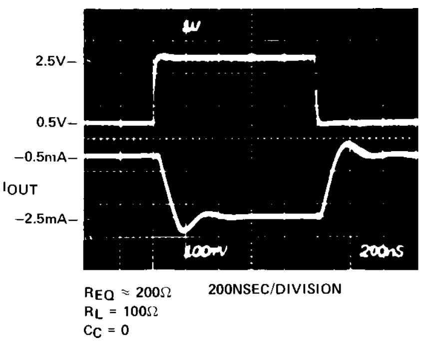


Figure 3. Fast Pulsed Reference Operation

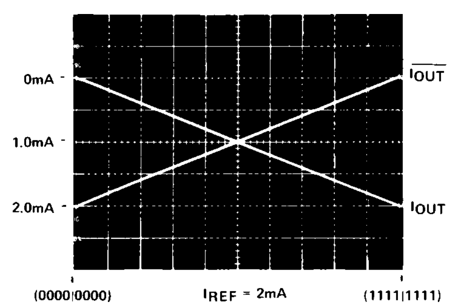


Figure 4. True and Complimentary Output Operation

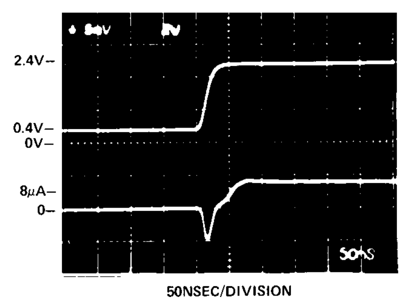


Figure 5. LSB Switching

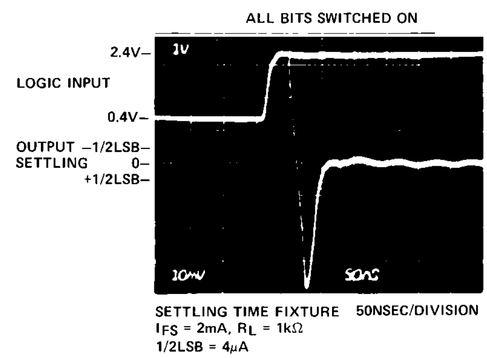


Figure 6. Full-Scale Settling Time

DAC08–Typical Performance Characteristics

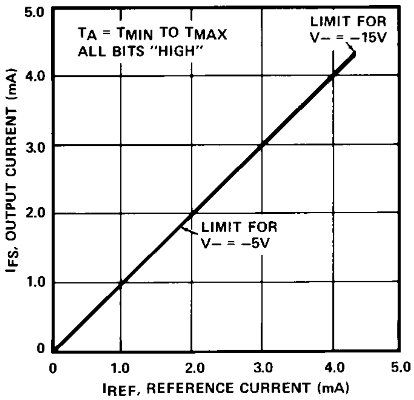


Figure 7. Full-Scale Current vs. Reference Current

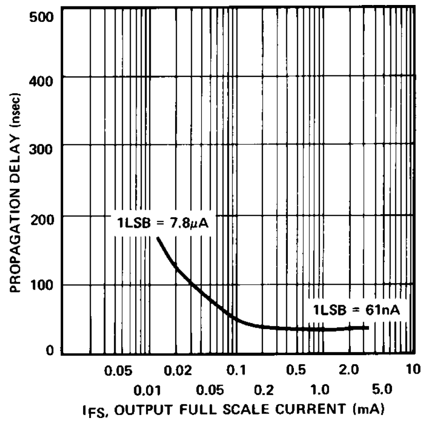


Figure 8. LSB Propagation Delay vs. I_{FS}

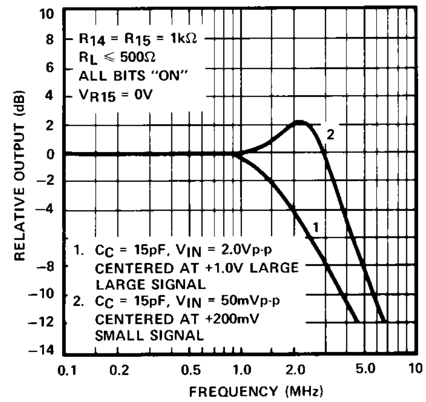


Figure 9. Reference Input Frequency Response

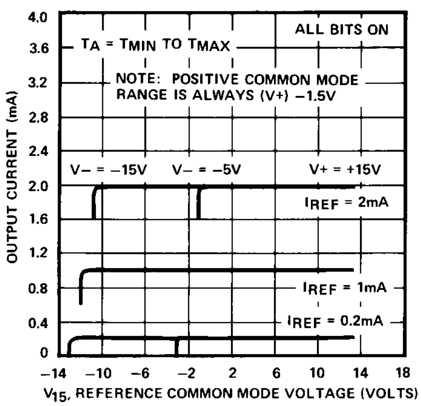


Figure 10. Reference Amp Common-Mode Range

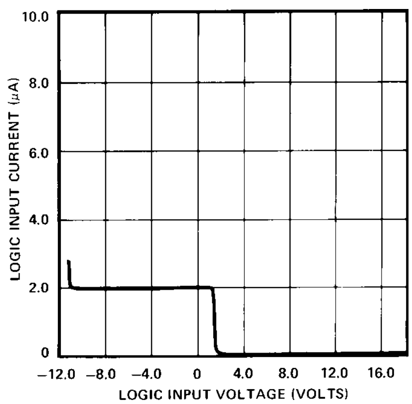


Figure 11. Logic Input Current vs. Input Voltage

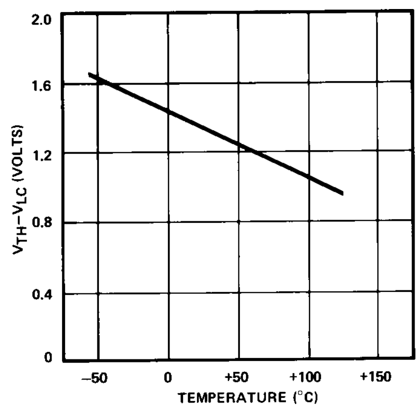


Figure 12. V_{TH}–V_{LC} vs. Temperature

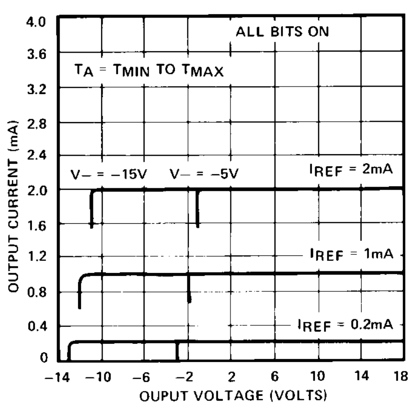


Figure 13. Output Current vs. Output Voltage (Output Voltage Compliance)

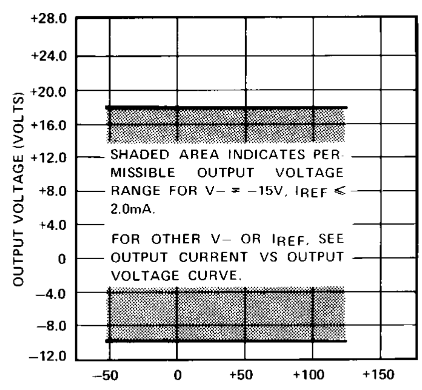


Figure 14. Output Voltage Compliance vs. Temperature

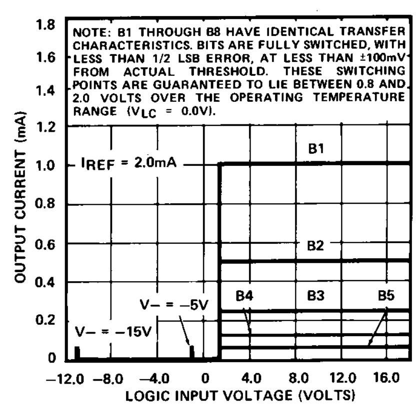


Figure 15. Bit Transfer Characteristics

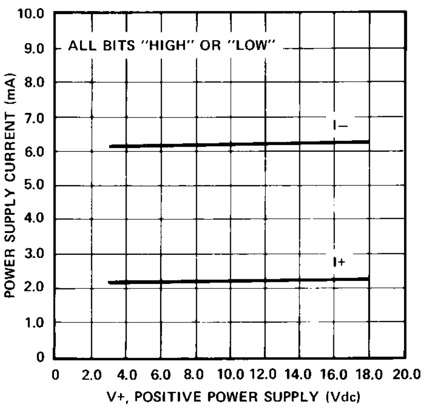


Figure 16. Power Supply Current vs. V+

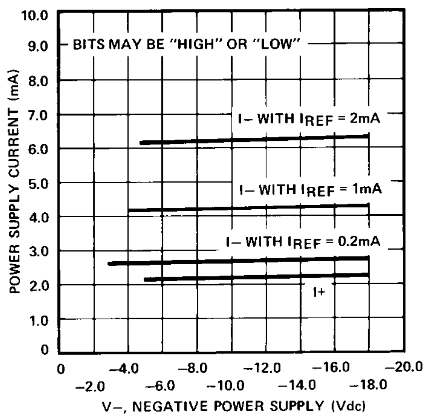


Figure 17. Power Supply Current vs. V–

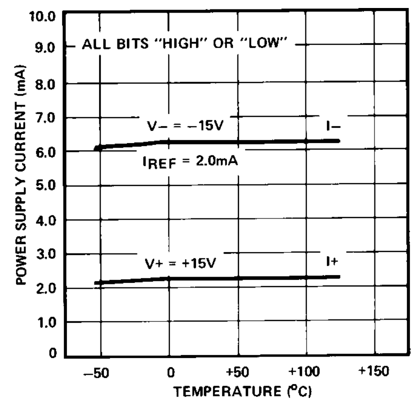


Figure 18. Power Supply Current vs. Temperature

BASIC CONNECTIONS

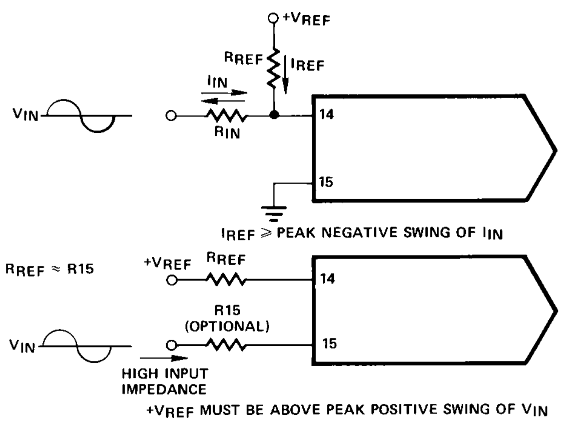


Figure 19. Accomodating Bipolar References

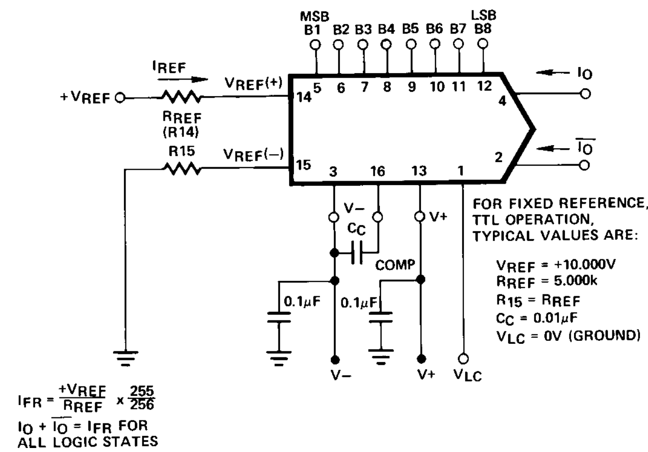
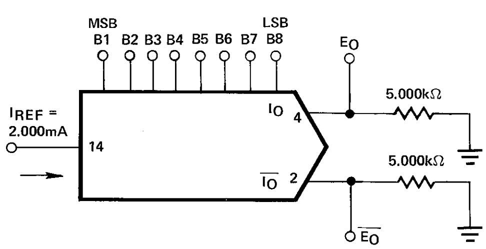
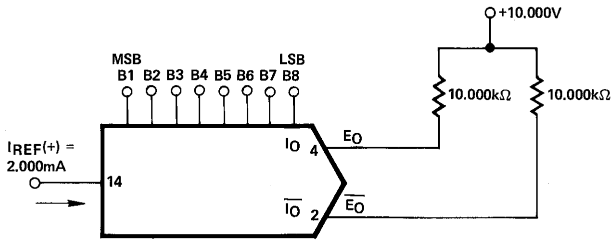


Figure 20. Basic Positive Reference Operation



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	0.000	–9.960	– .000
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008	0.984	–5.040	–4.920
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	0.992	–5.000	–4.960
HALF-SCALE –LSB	0	1	1	1	1	1	1	1	0.992	1.000	–4.960	–5.000
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	–0.040	–9.920
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	–9.960

Figure 21. Basic Unipolar Negative Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS. FULL RANGE	1	1	1	1	1	1	1	1	− 9.920	+10.000
POS. FULL RANGE −LSB	1	1	1	1	1	1	1	0	− 9.840	+ 9.920
ZERO-SCALE +LSB	1	0	0	0	0	0	0	1	− 0.080	+ 0.160
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO-SCALE −LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG. FULL-SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	− 9.840
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	+10.000	− 9.920

Figure 22. Basic Bipolar Output Operation

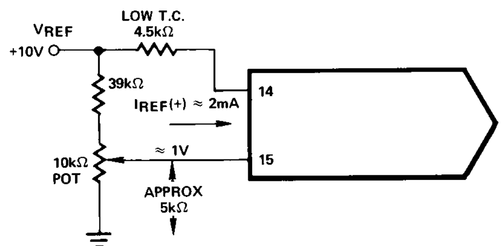


Figure 23. Recommended Full-Scale Adjustment Circuit

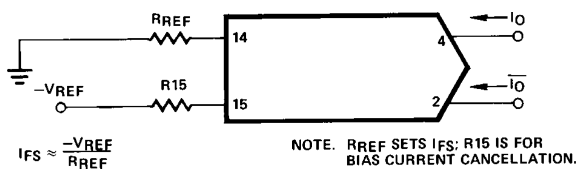
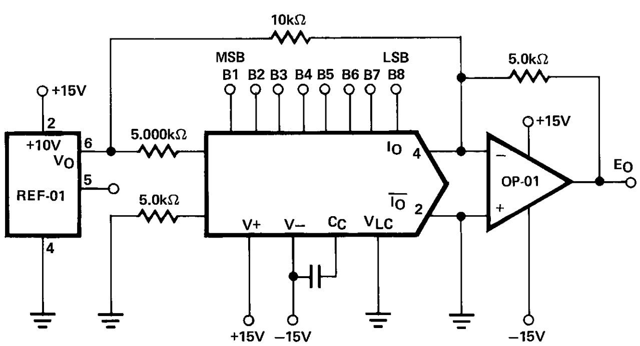
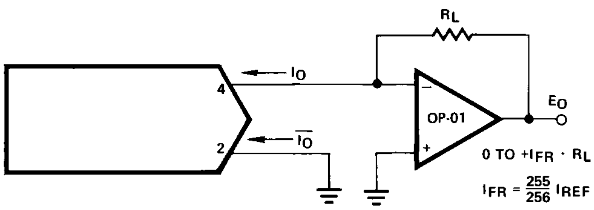


Figure 24. Basic Negative Reference Operation



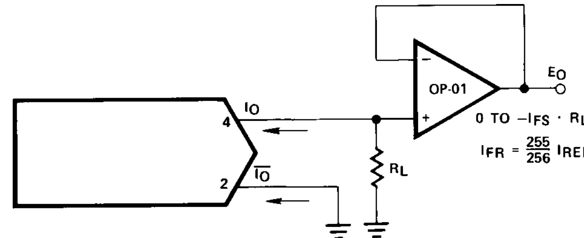
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS. FULL RANGE	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

Figure 25. Offset Binary Operation



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

Figure 26. Positive Low Impedance Output Operation



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NONINVERTING INPUT OF OP-AMP TO I_O (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

Figure 27. Negative Low Impedance Output Operation

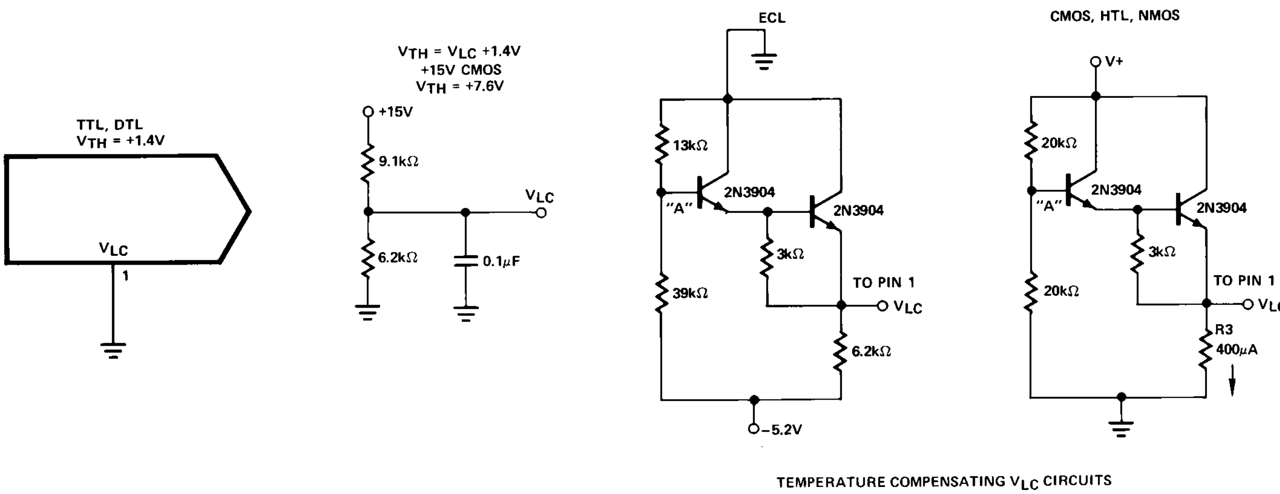


Figure 28. Interfacing With Various Logic Families

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SET-UP

The DAC08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0 mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors; R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM}– = V–$ plus ($I_{REF} \times 1$ kΩ) plus 2.5 V. The positive common-mode range is V+ less 1.5 V.

When a dc reference is used, a reference bypass capacitor is recommended. A 5.0 V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1 μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full-scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a dc reference current is +0.2 mA to +4.0 mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V–. The value of this capacitor depends on the impedance presented to pin 14: for R14 values of 1.0, 2.5 and 5.0 kΩ, minimum values of C_C are 15, 37, and 75 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin, such that the ratio of C_C (pF) to R14 (kΩ) = 15.

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1 kΩ and C_C = 15 pF, the reference amplifier slews at 4 mA/µs enabling a transition from I_{REF} = 0 to I_{REF} = 2 mA in 500 ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 mA to 2 mA) occurs in 120 ns when the equivalent impedance at pin 14 is 200 Ω and C_C = 0. This yields a reference slew rate of 16 mA/µs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2 µA logic input current and completely adjustable logic threshold voltage. For V– = –15 V, the logic inputs may swing between –10 V and +18 V. This enables direct interface with +15 V CMOS logic, even when the DAC08 is powered from a +5 V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus (I_{REF} × 1 kΩ) plus 2.5 V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1 mA is recommended. For interfacing other logic families, see preceding page. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100 µA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1 kΩ divider, for example, it should be bypassed to ground by a 0.01 µF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" (I_O) output when a "1" (logic high) is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36 V above V– and is independent of the positive supply. Negative compliance is given by V– plus (I_{REF} × 1 kΩ) plus 2.5 V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC08 operates over a wide range of power supply voltages from a total supply of 9 V to 36 V. When operating at supplies of ±5 V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –4.5 V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8 V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

P_d = (I+) (V+) + (I–) (V–). A useful feature of the DAC08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically ±10 ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC08 decrease approximately 10% at –55°C; at +125°C an increase of about 15% is typical.

The reference amplifier must be compensated by using a capacitor from pin 16 to V–. For fixed reference operation, a 0.01 µF capacitor is recommended. For variable reference applications, see previous section entitled "Reference Amplifier Compensation for Multiplying Applications".

MULTIPLYING OPERATION

The DAC08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4 mA to 4 mA. Monotonic operation is maintained over a typical range of I_{REF} from 100 μA to 4.0 mA.

SETTLING TIME

The DAC08 is capable of extremely fast settling times, typically 85 ns at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35 ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35 ns, with each progressively larger bit taking successively longer. The MSB settles in 85 ns, thus determining the overall settling time of 85 ns. Settling to 6-bit accuracy requires about 65 ns to 70 ns. The output capacitance of the DAC08 including the package is approximately 15 pF, therefore the output RC time constant dominates settling time if R_L > 500 Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4 μA, therefore a 1 kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture shown in schematic labelled "Settling Time Measurement" uses a cascode design to permit driving a 1 kΩ load with less than 5 pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0 mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 μF capacitors at the supply pins provide full transient protection.

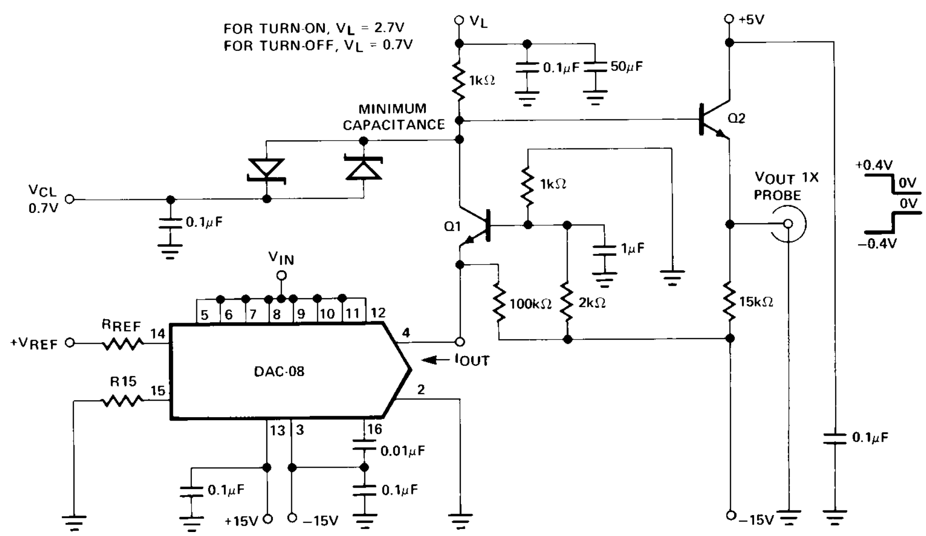
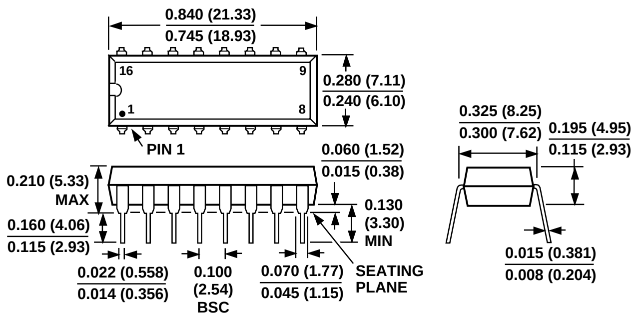


Figure 30. Settling Time Measurement

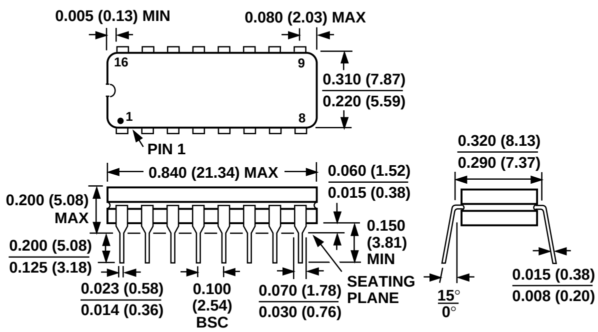
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

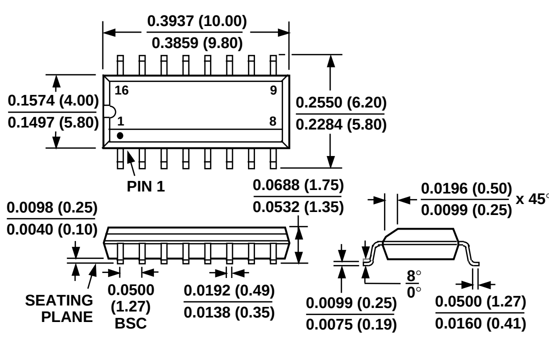
N-16



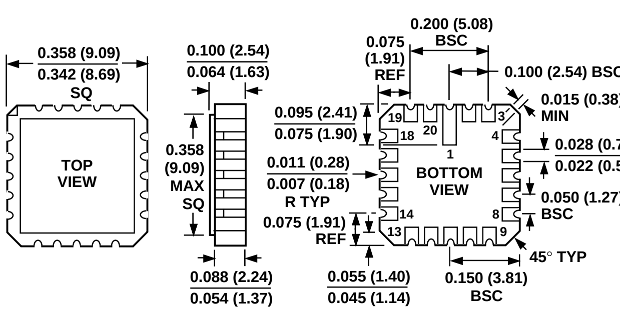
Q-16



SO-16



E-20



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